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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/938,093	08/23/2001	David J. Flynn	21220/04089 (GR201 SF054)	9854
24024	7590	11/03/2004	EXAMINER	
CALFEE HALTER & GRISWOLD, LLP 800 SUPERIOR AVENUE SUITE 1400 CLEVELAND, OH 44114			MISLEH, JUSTIN P	
			ART UNIT	PAPER NUMBER
			2612	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 09/938,093	<b>Applicant(s)</b> FLYNN, DAVID J.	
	<b>Examiner</b> Justin P Misleh	<b>Art Unit</b> 2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1 - 20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 - 11, 19, and 20 is/are rejected.
- 7) ☒ Claim(s) 11 - 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 August 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

## DETAILED ACTION

### *Specification*

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. **The form and legal phraseology often used in patent claims, such as “means”, “said” and “disclosed,” should be avoided.** The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, “The disclosure concerns,” “The disclosure defined by this invention,” “The disclosure describes,” etc.

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.
3. The disclosure is objected to because of the following informalities: The difference between two separate reference sign descriptions is unclear.

More specifically, reference sign 42 and reference sign 40 point to separate items in figure 2; however, in the specification, reference sign 40 is labeled as a CCD image detector and reference sign 42 is also labeled as a CCD image detector. The Examiner suggests amending the

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specification, at all appropriate instances, to clearly distinguish between each reference sign as they are distinguished in figure 2.

Appropriate correction is required.

### ***Drawings***

4. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).

Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

5. **Claim 11** is objected to because of the following informalities: lack of clarity and precision.

In regards to step (b), the Applicant states "a burst of first clock pulses wherein each said pulse controls", and likewise, in regards to step (c), the Applicant states "a burst of second clock pulses wherein each said pulse controls". Due to the fact that in both steps (b) and (c), the Applicant simply states "said pulse controls" demonstrates a lack of clarity and precision, because the Applicant fails to specify which "said pulse controls" the Applicant intended to refer

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to. To alleviate the problem, the Examiner suggests changing “said pulse controls” to “said first pulse controls” and “said second pulse controls”, respectively. For the purposes of examination, the Examiner will interpret Claim 11 according to the above-stated suggestions.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. **Claims 1, 2, 4, 5, 7 – 10, 11, and 20** are rejected under 35 U.S.C. 102(b) as being anticipated by David et al.

8. For **Claim 1**, David et al. disclose, as shown in figures 7 – 11 and as stated in columns 8 (lines 54 – 67), 9 (lines 1 – 11), and 11 (lines 10 – 42), a charge coupled device (CCD) image detector comprising:

an image area (500) of an array of rows of gates, each gate of said image area array being operative to collect and store a charge content representative of a picture element (pixel) of an image, said rows of gates of the image area being operative concurrently by a first clock signal ( $\phi_i$ ) to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in a predetermined direction through said image area;

a storage area (600/700) of array of rows of gates, each gate of said storage area array being operative to store a charge content, said rows of gates of the storage area being operative

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concurrently by a second clock signal ( $\phi_s$ ) to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through said storage area, said storage area array of rows (600/700) disposed in said CCD detector such that a first row of said image area array of rows (bottom-most row closest to the storage area 600/700) is adjacent a last row of said storage area array of rows (top-most row closest to the image area 500) to accommodate a transfer in parallel of the charge contents of the gates of said first row of the image area to the gates of said last row of the storage area (the solid single direction directional arrows are the direction in which charge travels), wherein the image and storage areas are operative by the first and second clock signals, respectively, to transfer the charge contents of the rows of the image area array to rows of the storage area array (See figure 9 and column 9, lines 1 – 11);

a buffer area (610/710) of an array of rows of gates, each gate of said buffer area array being operative to store a charge content, said rows of gates of the buffer area being operative concurrently by a third clock signal ( $\phi_b$ ) to transfer in parallel the charge contents of the gates of each row to the gates of an adjacent row in the predetermined direction through said buffer area, said buffer area array of rows disposed in said CCD detector such that a first row of said storage area array of rows (bottom-most row closest to the buffer area 610/710) is adjacent a last row of said buffer area array (top-most row closest to the storage area 600/700) of rows to accommodate a transfer in parallel of the charge contents of the gates of said first row of the storage area to the gates of said last row of the buffer area, wherein the storage and buffer areas are operative by the second and third clock signals, respectively, to transfer the charge contents of the rows of the storage area array to rows of the buffer area array (See figure 9 and column 9, lines 1 – 11); and

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a readout register (340) of a row of gates, each gate of said readout register being operative to store a charge content, said readout register disposed in said CCD detector such that a first row of said buffer area array (bottom-most row closest to the readout register 340) of rows is adjacent the row of said readout register (340) to accommodate a transfer in parallel of the charge contents of the gates of said first row of the buffer area to the gates of said readout register as controlled solely by the third clock signal (the clock signals operate independently), said row of gates of the readout register being operative concurrently by a fourth clock signal ( $\phi_h$ ) to transfer serially the charge contents of the gates thereof through said register in a predetermined direction to an output signal line (350).

9. As for **Claim 2**, David et al. disclose, as shown in figures 7 and 10, the CCD image detector of Claim 1 wherein the number of rows (1035 – rows) of the image area array (500) is equal to the composite number of rows of the storage area array (600/700 – 748 rows) and buffer area array (610/710 – 287 rows).

10. As for **Claim 4**, David et al. disclose, as stated in columns 8 (lines 59 – 65) and 11 (lines 25 – 31), that the number of rows in the buffer area (610/710) is purposely set as a fraction of the number of rows of the image area (500), so as to achieve the advantages of a reduction in “thermal noise” and increased “bandwidth”; therefore, David et al. also disclose the CCD image detector of Claim 1 wherein the number of rows of the buffer area array (610/710) is equal to the number of a designated band of rows of the image area array.

11. As for **Claim 5**, although it is not shown, it is inherent to David et al. for David et al. to provide the CCD image detector of Claim 1 comprising a timing controller for controlling the

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operation of the first, second, third and fourth clock signals. David et al. would not be able to provide the clock signals ( $\phi_i$ ;  $\phi_s$ ;  $\phi_b$ ;  $\phi_h$ ) if a timing controller were not present therein.

12. As for **Claim 7**, David et al. disclose, as shown in figure 9, the CCD image detector of Claim 5 wherein the timing controller operates the first, second, third and fourth clock signals ( $\phi_i$ ;  $\phi_s$ ;  $\phi_b$ ;  $\phi_h$ ) in a predetermined sequence to effect a readout of the charge content of a plurality of bands (one band of a plurality of bands corresponds the “previous active field period” and another band of the plurality of bands corresponds to the “field period”) of rows of gates.

13. As for **Claim 8**, David et al. disclose, as shown in figures 10 and 11, the CCD image detector of Claim 5 wherein the timing controller operates the first, second, third and fourth clock signals ( $\phi_i$ ;  $\phi_s$ ;  $\phi_b$ ;  $\phi_h$ ) in a predetermined sequence to effect a readout of the charge content of an image frame (“frame transfer”).

14. As for **Claim 9**, David et al. disclose, as shown in figure 9 and as stated in column 9 (lines 4 – 9), the CCD image detector of Claim 5 wherein timing controller is operative to:

(1 – see figure 9f) control the first, second and third clock signals ( $\phi_i$ ;  $\phi_s$ ;  $\phi_b$ ) concurrently to transfer the charge contents of the rows of the image area array to rows of the storage area array (600/700) and the buffer area array (610/710),

(2 – see figure 9b) control the second and third clock signals ( $\phi_s$ ;  $\phi_b$ ) concurrently to transfer the charge contents of the rows of the storage area array (600/700) to rows of the buffer area array (610/710),

(3 – see figure 9d) control the third clock signal ( $\phi_b$ ) to transfer in parallel the charge contents of the last row of the buffer area (610/710) to the readout register (340), and



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(4 – see column 9, lines 4 – 9) control the fourth clock signal ( $\emptyset h$ ) to transfer serially the charge contents of the gates of the readout register (340) through the register in a predetermined direction to the output signal line (350).

15. As for **Claim 10**, David et al. disclose, as shown in figures 7, 8, and 9 and as stated in column 9 (lines 4 – 9), the CCD image detector of Claim 5 wherein the timing controller controls solely the third clock signal ( $\emptyset b$ ) to transfer the charge contents of the buffer area array (610/710) of rows to the read out register (340).

16. For **Claim 11** (please see objection above), David et al. disclose, as shown in figures 7 – 11 and as stated in columns 8 (lines 54 – 67), 9 (lines 1 – 11), and 11 (lines 10 – 42), method of operating a charge coupled device (CCD) as an image detector comprising the steps of:

(a – see figures 9a – 9c) collecting and storing charge content in gates of an image area array (500) of rows of gates for a predetermined period of time, said charge content of said gates of said image area array representative of a picture elements (pixels) of an image frame;

(b – see figures 9d – 9f) transferring the stored charge contents of the image area array (500) to a storage area array (600/700) of rows of gates controlled by a burst of first clock pulses ( $\emptyset i$  – see column 8, lines 54 – 60, and column 10, lines 16 – 20) wherein each said [first] pulse controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the image and storage areas in a predetermined direction (the solid single direction directional arrows are the direction in which charge travels);

(c – see figures 9f and 9g) transferring the charge contents of a predetermined number of adjacent rows of the storage area array (600/700) to a like number of adjacent rows of a buffer area array (610/710) of rows of gates controlled by a burst of second clock pulses ( $\emptyset s$  – see

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column 10, lines 32 – 40) wherein each said [second] pulse controls the transfers in parallel of the stored charge contents of gates between adjacent rows through the storage and buffer areas in the predetermined direction (the solid single direction directional arrows are the direction in which charge travels);

(d – see figures 9a – 9c) transferring in parallel the charge contents of adjacent rows through the buffer area array (610/710) in the predetermined direction by a pulse of a third clock ( $\phi_b$ ) so that the charge contents of a last row of gates of the buffer area array are transferred in parallel to a row of gates in a readout register (340);

(e – see column 9, lines 4 – 9) shifting out the charge contents of the gates of the readout register serially to an output (350) of the CCD as controlled by the pulses of a fourth clock ( $\phi_h$ );

(f) thereafter, repeating steps (d) and (e) for each row of the predetermined number of adjacent rows of stored charge content of the buffer area array transferred from the storage area array in step (d); and

(g) repeating steps (c)-(f) for each predetermined number of adjacent rows of a set of predetermined number of adjacent rows of the storage area array (Steps f and g correspond to a frame transfer method of operating, which is shown in figures 10 and 11 of David et al.).

17. As for **Claim 20**, David et al. disclose, as shown in figures 9 and 10, a “previous field” and a current “field”; therefore, David et al. disclose the method of Claim 11 including the step of repeating steps of (a) through (g) periodically.

***Claim Rejections - 35 USC § 103***

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

19. **Claims 3, 6, and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over

David et al.

20. As for **Claim 3**, David et al. disclose, as stated in columns 8 (lines 59 – 65) and 11 (lines 25 – 31), that the number of rows in the buffer area (610/710) is purposely set as a fraction of the number of rows of the image area (500), so as to achieve the advantages of a reduction in “thermal noise” and increased “bandwidth”; however, David et al. does not specify that the number of rows in the buffer area is equal to the square root of the number of rows of the image area rounded up to the nearest integer.

Since setting the number of rows in the buffer area to a specific fraction of the number of rows in the image area is taught by David et al., at the time the invention was made, it would have obvious to one with ordinary skill in the art to also have set the number rows in the buffer area to the square root of the number of rows of the image area rounded up to the nearest integer. At the time the invention was made, one with ordinary skill in the art would have been motivated to set the number of rows in the buffer area to the square root of the number of rows of the image area rounded up to the nearest integer for the advantage of reducing the “thermal noise” and increasing the “bandwidth” of image data.

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21. As for **Claims 6 and 19**, while David et al. disclose operating the CCD image detector as a frame transfer image detector, David et al. do not disclose purging the CCD image detector of charge contents. However, Official Notice (See MPEP § 2144.03) is taken that both the concepts and advantages of purging the CCD image detector of charge contents are well known and expected in the art. At the time the invention was made, it would have been obvious to one with ordinary skill in the art to have purged the CCD image detector of charge contents, so as to reduce the occurrence of smearing.

***Allowable Subject Matter***

22. **Claims 12 – 18** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

As for **Claims 12 and 15**, while the closest prior art teaches of providing a frame transfer charge-coupled image sensor wherein the transfer rate between an image acquisition area and an image storage is low to reduce thermal and fixed pattern noise, the closest prior art does not teach or fairly suggest dividing the storage area array into a plurality of bands of rows wherein each band of said plurality includes a predetermined number of adjacent rows of charge content and then transferring the charge contents of a predetermined number of adjacent rows of the storage area array to a like number of adjacent rows of a buffer area array of rows of until a first band of charge content of said plurality of bands is transferred to the buffer area array.

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***Conclusion***

23. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following is a brief description of the cited prior art as labeled on attached form PTO-892:

- **Prior Art B** discloses, in the very least, as shown in figure 3, an image area array (24), storage area array (26A), a buffer area array (26B), and a readout register (27).

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Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 703.305.8090. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 5:30 PM and on alternating Fridays from 7:30 AM to 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wendy R Garber can be reached on 703.305.4929. The fax phone number for the organization where this application or proceeding is assigned is 703.872.9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM

October 21, 2004

  
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